Paper No. ____

Filed on behalf of: Senior Party Lofgren

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES
(Administrative Patent Judge Lee)

KATO et al.
(Patent 6,538,926)
Junior Party

v.

LOFGREN et al.
(Application 10/809,061)
Senior Party.

Patent Interference No. 105,567 (JL)
(Technology Center 2800)

FILING OF AMENDMENT

In accordance with the authorization given in Judge Lee's "Order—Not Authorizing Motions – Bd.R. 104(a)" dated September 12, 2007, Senior Party Lofgren hereby files the accompanying Amendment to its application no. 10/809,061 involved in the present interference. This Amendment substitutes the term "shift register" for each occurrence of "buffer memory" in the application's claims.

Pursuant to Judge Lee's request during the telephone conference of September 11, 2007, a copy of this Amendment was sent to counsel for Junior Party Kato on September 11, 2007 for comments as to form but no response has yet been received by counsel for Senior Party Lofgren.

Dated: September 12, 2007

Respectfully submitted,

/Gerald P. Parsons/

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Attorney Docket No.: SNDK.557US0

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Karl M.J. Lofgren et al.		
Title:	Device and Method for Controlling Solid-State Memory System		
Application No.:	10/809,061	Filing Date:	March 24, 2004
Examiner:	Mai, Son Luu	Group Art Unit:	2827
Docket No.:	SNDK.015US7	Conf. No.:	6999

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT

Sir:

This Amendment is being filed as the result of a Telephonic Hearing held on September 11, 2007, in Patent Interference No. 105,567 (JL), in which the present application is involved.

Amendments to the Claims are given in the Listing of the Claims beginning on page 2 of this paper.

Remarks begin on page 5 of this paper.

AMENDMENTS TO THE CLAIMS

Please amend claims 40, 48, 51, and 54 as indicated below.

LISTING OF CLAIMS

Claims 1-39: (Cancelled.)

40.(Currently Amended) A nonvolatile memory system comprising:

a nonvolatile memory including a plurality of nonvolatile memory cells and a ~~buffer memory~~ shift register; and

a control device coupled to said nonvolatile memory, wherein said control device is enabled to receive data from outside of said nonvolatile memory system and to apply said data to said nonvolatile memory,

wherein said nonvolatile memory is enabled to operate a program operation,

wherein in said program operation, said nonvolatile memory receives said data from said control device, stores said data to said ~~buffer memory~~ shift register and stores said data in said ~~buffer memory~~ shift register to ones of said nonvolatile memory cells,

wherein said control device is enabled to receive data from outside of said nonvolatile memory system, while said nonvolatile memory is operating in said program operation, and

wherein said ~~buffer memory~~ shift register has a data storing capacity enabling the transfer of a unit of data of a length equal to the data length of said data to be stored at one time of said program operation, said data length being more than 1 byte.

Claims 41-46: (Cancelled.)

47.(Previously Presented) A nonvolatile memory system according to claim 40,

wherein said nonvolatile memory includes a plurality of word lines and a plurality of data lines, and wherein each of said nonvolatile memory cells is arranged at a crossing point of a corresponding one of said word lines and a corresponding one of said data lines and is coupled to the corresponding word line and corresponding data line.

48.(Currently Amended) A nonvolatile memory system according to claim 47,

wherein said nonvolatile memory includes a plurality of sectors each comprising one word line and ones of the nonvolatile memory cells coupled thereto, and wherein said ~~buffer memory~~ shift register has a data storing capacity enabling the receiving of a unit of data of a length equal to the data storing capacity and enabling the storing of a unit of data in said sector.

49.(Previously Presented) A nonvolatile memory system according to claim 48, wherein said nonvolatile memory is a flash memory.

50.(Previously Presented) A nonvolatile memory system according to claim 40,

wherein said control device includes a host interface comprised of a data bus transceiver, an address bus driver, an address decoder and a control bus controller, to enable communication between the nonvolatile memory and an external system bus.

51.(Currently Amended) A nonvolatile memory system comprising:

a plurality of nonvolatile memories each including a plurality of nonvolatile memory cells and a ~~buffer memory~~ shift register; and

a control device coupled to said nonvolatile memories, wherein said control device is enabled to receive data from outside of said nonvolatile memory system and to apply said data to said nonvolatile memories,

wherein said nonvolatile memories are enabled to operate a program operation,

wherein in said program operation, each of said nonvolatile memories selectively receives said data from said control device, stores said data to said ~~buffer memory~~ shift register thereof and stores said data in said ~~buffer memory~~ shift register to ones of said nonvolatile memory cells of that nonvolatile memory,

wherein said control device is enabled to receive data from outside of said nonvolatile memory system, while said nonvolatile memories are operating in said program operation, and

wherein said ~~buffer memory~~ shift register has a data storing capacity enabling the transfer of a unit of data of a length equal to the data length of said data to be stored at one time of said program operation, said data length being more than 1 byte.

Claim 52: (Cancelled.)

53.(Previously Presented) A nonvolatile memory system according to claim 51,

wherein each of said nonvolatile memories further includes a plurality of word lines and a plurality of data lines, and

wherein each of said nonvolatile memory cells in each of the nonvolatile memories is arranged at a crossing point of a corresponding one of said word lines and a corresponding one of said data lines and is coupled to said corresponding word line and corresponding data line.

54.(Currently Amended) A nonvolatile memory system according to claim 53,

wherein each of said nonvolatile memories includes a plurality of sectors each comprising one word line and ones of the nonvolatile memory cells coupled thereto, and

wherein said ~~buffer memory~~ shift register has a data storing capacity for receiving data in units of a sector and enabling the storing of a unit of data in said sector.

55.(Previously Presented) A nonvolatile memory system accordance to claim 54,

wherein each of said nonvolatile memories is a flash memory.

56.(Previously Presented) A nonvolatile memory system according to claim 55,

wherein said control device includes a host interface comprised of a data bus transceiver, an address bus driver, an address decoder and a control bus controller, to enable communication between the nonvolatile memories and an external system bus.

57.(Previously Presented) A nonvolatile memory system according to claim 51,

wherein said control device includes a host interface comprised of a data bus transceiver, an address bus driver, an address decoder and a control bus controller, to enable communication between the nonvolatile memories and an external system bus.

REMARKS

This amendment is being filed in order to conform with the discussion in the Telephonic Hearing in Patent Interference Number 105,567 (JL) before Administrative Patent Judge Jamison Lee on September 11, 2007.

Respectfully submitted,

/Gerald P. Parsons/ September 12, 2007
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